Abstract of the Disclosure

A memory cell array block has unit memory cells comprised of pairs of memory cells, each of have a memory cell and a complementary memory cell.. A second unit memory cell is interleaved with the first unit memory cell, a fourth unit memory cell is interleaved with a third unit memory cell. First and second sense amplifiers are disposed over and under the array block, respectively. The first switch connects bitlines coupled to the first unit memory cell with the first sense amplifier and connects bitlines coupled to the second unit memory cell with the second sense amplifier. The second switch connects bitlines coupled to the third unit memory cell with the first sense amplifier and connects bitlines coupled to the fourth unit memory cell with the second sense amplifier. A selected unit memory cell is selectively connected with a sense amplifier, decreasing the number of sense amplifiers.